Remarks/Arguments:

Claims 1-26 are pending in the present application. New claim 26 has been added to enhance the scope of Applicant's patent coverage. The support for new dependent claim 26 is found in Figure 5 of Applicant's disclosure. In the Office Action dated August 24, 2005, the PTOL-326 indicates that the Patent Office has allowed claims 14-19, and rejected claims 11-13 only under 35 U.S.C. 112, 2nd Paragraph. Applicant appreciates the indication of allowability by the Patent Office. The Office Action further rejected claims 1-2 as obvious under 35 U.S.C. 103(a) as being unpatentable over an article by Cox et al., has rejected claims 1-6 under 35 U.S.C. 103(a) as being unpatentable over an article by Kim et al., and has rejected claims 1, 2, 4-10, and 20-25 under 35 U.S.C. 103(a) as being unpatentable over Mantha, U.S. Published Patent Application No. 2003/0126551.

The Patent Office objected to the specification for informalities. Amendments have been made adopting the Patent Office's suggestions in the first paragraph of the objections to the specification section.

Regarding the second paragraph, "puncturing sequences." For each code rate supported, both the transmitter and the receiver must have information as to puncture locations beforehand. Both the transmitter and the receiver store the LDPC mother code definition 37B and a puncturing sequence 35B that can be used, in whole or in part, for any of the different code rates. In Applicant's invention, the locations of these P punctures are a contiguous subset selected from a single puncture sequence S_{N-K} of length (N-K). Both the transmitter and receiver store the same predetermined sequence for a given LDPC mother code in memory. For the code rate $K/(N-P)$, each terminal would then use the first P elements of the same S_{N-K} puncture sequence for the mother codeword. Regarding "degrees," either variable degrees or variable node locations in the codeword compose the individual elements of the puncture sequence S_{N-K} if the communication system strictly bounds the maximum code rate below one. In Figs. 1A and 1B, the number of variable edges 30 connected to a particular variable node 26 is termed its degree, and the number of variable degrees 32 are shown corresponding to the number of variable edges 30 emanating from each variable node 26. Regarding puncturing sequences, Applicant has defined in the background of the invention Applicant's understanding of the prior art. Besides substantial amounts of memory required to store prior art puncturing sequences for various coding rates, the determination of the puncturing sequences is itself computationally intensive. Like the coding systems themselves, the prior art reveals at least two distinct methods for designing a

puncture sequence. The first method is based on linear programming to determine puncturing probabilities that maximize the puncturing fraction:

$$p^{(0)} = \sum_{j=2}^{d_l} \lambda'_j \pi_j^{(0)}$$

for a given signal to noise ratio (SNR, or bit/symbol energy to noise power spectral density E_b/N_0) threshold, wherein λ'_j represents the fraction of variable nodes 26 of degree j. The other prior art approach to puncture sequence design is based on differential evaluation based on Density Evolution, which is somewhat more complex than the linear programming method described immediately above with near identical results. Each of these approaches for designing the puncture sequences are very computationally expensive, and their resulting sequences themselves require so much storage as to be potentially prohibitive for an adaptive coding system. Applicant describes the maximum puncture sequence as represented by a relatively long sequence of memory elements 54, which are depicted as sequential but need not be stored in physically adjacent areas of a volatile memory. A first puncture sequence S_1 is stored at a first memory element 54a, which is the first memory element of the sequence of memory elements that comprise the maximum rate puncture sequence S_{N-K}. In terms of the matrix **H** of Figure 1A, the first puncture sequence may represent either the non-zero element locations (variable node locations) or the number of non-zero elements (variable degree) of the first column. A second puncture sequence S_2 is stored at a first 54a and second 54b memory elements, which are the first two memory elements of the sequence of memory elements that comprise the maximum rate puncture sequence S_{N-K}. In terms of the matrix **H** of Figure 1A, the second puncture sequence may represent either the non-zero element locations (variable node locations) or the number of non-zero elements (variable degree) of the first and second columns. By this arrangement, S_1 is a subset of S_2, which is a subset of S_3, etc., and all are subsets of S_{N-K}. This relation is written as $S_1 \subseteq S_2 \subseteq S_3 \subseteq \ldots \subseteq S_{N-K}$. Both the transmitter and receiver store the same predetermined sequence for a given LDPC mother code in memory. Regarding the last sentence in the second paragraph of commentary of section 1, Applicant's disclosure has not limited itself to parity bits as the only bits that are punctured. Applicant believes that the present disclosure as originally filed has sufficient clarity to teach one or ordinary skill in the art to make and/or use Applicant's invention. Applicant thus requests that the Patent Office withdraw its objections to the specification.

The Patent Office rejected claims 1-13 and 20-25 under 35 U.S.C. 112, Second Paragraph. The amendment to claims 1, 4, 11, 12, 20 and 23 should overcome the rejection made under 35 U.S.C. 112, Second Paragraph.

The Patent Office rejected claims 1-6 under 35 U.S.C. 103(a) as being unpatentable over Kim.

Claim 1 recites "A communication unit for a multiple code rate communication system comprising a codeword defining N codeword elements and K information elements coded at a code rate R=K/(N-P), wherein P is a number of punctured elements of the codeword; a first storage location for storing an error reduction code mother code definition; a second storage location for storing a maximum puncture sequence S_{max}, wherein S_{max} is the puncture sequence for a maximum code rate R_{max}, and further wherein **S_{max} comprises a subset S_1 that is a puncture sequence for a minimum code rate R_1.**"

Claims 1-6 are not amended, except for clarification matters, and are seen to patentably distinguish over the references in light of the following remarks. Kim will be considered first as it is seen to provide more relevant detail.

Kim is directed to a rate compatible punctured serial concatenated convolutional code SCCC. In that Kim describes varying both an inner and an outer code (serial concatenation) to achieve a variable rate code, new claims 20-25 are seen to distinguish in that each recites an encoder or decoder that encodes or decodes at a variable rate. See Kim, Fig. 1(a) for outer and inner encoders. Whereas Kim recites at page 2400, right-hand column, first paragraph that only a single rate encoder and decoder is used for variable coding rates, this statement is seen to apply to both the inner and outer encoder separately, so both the transmitter and the receiver each use an inner and separate outer encoder/decoder to achieve the variable rate codes. Were it otherwise, the code would not be concatenated. The two encoders/decoders are not seen as combinable with ordinary skill because the outer code is interleaved prior to application of the inner code. See Kim, Fig. 1(b). This is described particularly at Kim, page 2400, left-hand column, under the subtitle "*A. Overview of SCCC*".

More fundamentally, the Office Action appears to rely on Kim's description of a puncturing table, shared by the transmitter and receiver, as teaching that the puncture table is used to achieve a maximum code rate and a subset of it is used to achieve a minimum code rate. The Applicant contends that this is not what Kim teaches or describes. Kim recites at page 2400 that

> "The puncturing table consists of the systematic and parity sub-blocks each having P bits, where the two sub-blocks specify the puncturing patterns for the systematic and parity components, and P stands for the puncturing period. For **each** puncturing index k_s, we define an n_l x P binary puncturing table, PT_{ks}, where puncturing index k_s=0, 1, ...$(n_l$-1$)P$ that can be set according to channel conditions." (boldface added).

As the index k_s gives the coding rate R_{ks}, this is seen to describe a different puncturing table PT_{ks} for each different rate R_{ks}.

Kim's Fig. 2 bears this out. Four tables are shown, each having four entries for systematic bits and four entries for parity bits, and each puncturing table associated with a different coding rate. The highest coding rate is seen as R_0=2/3, associated with puncture table PT_0 that shows systematic bits 1, 1, 1, 1, and parity bits 0,0,0,0. All other rates are less than R_0=2/3 and vary from 8/15 to 1/3. For no other rate is the associated puncture table a subset of table PT_0 as the Office Action appears to assert in its rejection of claim 1. This is true even though the systematic bits are identical among the illustrated tables, because the parity bits of no other table is a subset of the parity bits of table PT_0. Kim is seen to teach storing different puncture tables for a variety of coding rates.

The approach of Kim is seen to follow that generally described at page 4, lines 2-9 of the written description, where a different LDPC code (the lower row of Kim's puncture tables) is designated for each coding rate and channel (Kim adapts coding rate to adapt to a time varying channel at page 2399, right-hand column). The present application notes shortfalls with this approach at page 4, lines 6-9 and line 2 to page 5, line 7, in that it requires a large volume of storage for long codewords, and is computationally expensive.

In contradistinction, claim 1 recites that the puncture sequence S_1 for a minimum code rate is a subset of the puncture sequence S_{max} for a maximum code rate. There is no need to store multiple tables for multiple code rates; a single table may be stored and lesser code rates taken from a subset of the single (maximum rate) table. Kim is not seen to disclose, teach, or suggest that an overall table may be used from which puncture sequences for lesser rates are a subset. Kim explicitly teaches away from such a modification at Fig. 2 by disclosing puncture tables for less than a maximum rate code that is not a subset of a puncture table PT_0 for his maximum rate code R_0=2/3. Even assuming arguendo that the various puncture tables of Kim may be accumulated into a conglomerate table, of which portions (the disclosed tables) are used selectively for various coding rates, Kim is not seen to use such a hypothetical conglomerate table to achieve a maximum coding rate. Claim 1 recites that the

puncture sequence for a minimum code rate is a subset of the puncture sequence for the maximum code rate.

Furthermore, claim 1 recites "S_{max} comprises a subset S_1 that is a puncture sequence for a minimum code rate R_1." Figure 2, on page 2401, of Kim, shows entries in a table. At best, each entry may be considered a sequence. The entries bear no relation to each other than as being different components of the table in which systematic and parity entries of four bits each are assigned to a certain code rate. There are no subsets of sequences taught or suggested by Kim. Thus, Kim does not make obvious claim 1.

The taking of Official Notice by the Patent Office is challenged. The Patent Office is requested to provide a reference supporting the material and motivation asserted as part of the Official Notice in the paragraph at the bottom of page 6 of the Office Action mailed August 24, 2005.

As to claim 4, Kim does not teach or suggest subsets. Thus, Kim does not make obvious claim 4.

As to claims 5 and 6, Kim discloses puncture table entries (Figure 2) that each contain the same number of bits as other entries and does not make obvious either claim 5 or claim 6.

The Patent Office rejected claims 1 and 2 under 35 U.S.C. 103(a) as being unpatentable over Cox.

Cox is seen to take the same general approach as Kim. Cox recites at page 1724 two puncturing tables $a(1)$ and $a(2)$ [equations (17) and (18)] that are used to puncture a ½ rate convolutional mother code and achieve a resulting rate of 4/5 and 2/3, respectively. As with Kim, neither of the puncturing tables are subsets of the other. The few overlapping elements used for rate compatibility do not render the entire sequence (or table) a subset of the other. Cox is seen to suffer the same shortfalls respecting memory usage and computational/processing complexity that are described in the application and noted above with respect to Kim.

For the above reasons, claims 1, 5 and 6 are seen to patentably distinguish in their own right over both Kim and Cox as modified by ordinary skill noted in the Office Action. Claims 2-4 are seen as patentable for their dependence on claim 1.

The Patent Office rejected claims 1, 2, 4-10, and 20-25 under 35 U.S.C. 103(a) as being unpatentable over Mantha, U.S. Published Patent Application No. 2003/0126551.

Claim 20 recites "A transmitter comprising an information source for providing a codeword; **a memory for storing a low density parity check code LDPC mother code definition** and a maximum puncture sequence S_{max}; a LDPC encoder having an input coupled

to an output of the information source and an input coupled to an output of the memory; and a modulator having an input coupled to an output of the LDPC encoder, wherein the encoder operates in one instance to encode at a maximum rate R_{max} by puncturing elements of a codeword in locations described by the maximum puncture sequence S_{max} read from the memory, and in another instance to encode at a lesser rate R_1 by puncturing elements of a codeword in locations described by **a subset S_1 of the maximum puncture sequence S_{max}** read from the memory."

Claim 23 recites "A receiver comprising a demodulator for demodulating a received codeword; **a memory for storing a low density parity check code LDPC mother code definition** and a maximum puncture sequence S_{max}; and a LDPC decoder having an input coupled to an output of the demodulator and an input coupled to an output of the memory; wherein the decoder operates in one instance to decode at a maximum rate R_{max} by de-puncturing elements of a codeword in locations described by the maximum puncture sequence S_{max} read from the memory, and in another instance to decode at a lesser rate R_1 by de-puncturing elements of a codeword in locations described by **a subset S_1 of the maximum puncture sequence S_{max}** read from the memory."

The Patent Office asserted (page 7 of the Office Action mailed August 24, 2005) "Mantha discloses an encoder for generating rate-compatibly punctured LDPCs, implemented by software. Each punctured LDPC codeword so generated is "a codeword defining N codeword elements and K information elements coded at a code rate R-K/(N-P), wherein P is a number of punctured elements of the codeword." The processes of generating the mother code (figure 1) and of subsequently puncturing the mother code (figure 2) are described by Mantha as being performed in two separate stages. Mantha describes the use of a puncturing table as "typical" [0136] and instead uses an algorithm based on two parameters in order to generate the puncturing patterns. Because the codes are punctured rate-compatibly, the puncturing patterns used by Mantha must be such that "S_{max} comprises a subset S_1 that is a puncture sequence for a minimum code rate R_1" [0127]."

Mantha (paragraph 0127) discloses "FIGS. 13 and 14 show serially concatenated systems. In FIG. 13, each new parity block P_1 is generated from the previously transmitted parity block P_{i-1} except of course P_1 , which is generated from the systematic information bits directly. All encoders 134a-134d and decoders 136a-136d can be identical. They can implement either turbo codes or LDPC codes. In FIG. 14 however, new parity blocks are generated in encoders 144a-144d from all previously transmitted bits. By using all previously transmitted bits, the code performance will improve, provided that the decoders

146a-performance [sic]. Additionally, any puncturing strategy must meet rate compatibility requirements. This means that at any particular code rate generated by puncturing, the parity bits involved must also be used by any lower rate code that might also be generated by puncturing."

Mantha discloses (regarding figure 1, paragraph 0059) "FIG. 1 depicts the type of channel considered in this disclosure. It is a discrete, memoryless channel. A discrete channel is defined as a system consisting of an input alphabet X and output alphabet Y and a probability transition matrix p(x|y) that represents the probability of observing the output symbol y given that the symbol x is transmitted. The channel is said to be memoryless if the probability distribution of the output depends only on the input at that time and is conditionally independent of previous channel inputs or outputs. These assumptions are justified because most modem communication systems operate on the basis of discrete symbol values."

Mantha, in paragraph 0136, discloses "An advantage to arbitrary puncturing is that a puncture mask for any puncturing amount can completely be described with just two numbers, the increment value δ and the initial value of the accumulator, σ_1 in FIG. 16. This means that the transmitter can inform the receiver (or vice versa) of the puncturing amount and hence code rate with a minimal exchange of information. This is in contrast with typical applications of puncturing, where the puncturing amounts are predetermined and stored in a lookup table in both the transmitter and the receiver." (Presumably, Kim represents a typical application.)

Mantha does not seem to disclose "S_{max} comprises a subset S_1 that is a puncture sequence for a minimum code rate R_1" or "a subset S_1 of the maximum puncture sequence S_{max}." Mantha also does not seem to suggest this limitation. Mantha also does not seem to disclose or suggest "a first storage location for storing an error reduction code mother code." As discussed above, Kim does not disclose or suggest these limitations. Thus, claims 1, 2, 4-10, and 20-25 are allowable over Mantha, alone or in combination with Kim.

As to claims 4-6, Mantha does not seem to teach or suggest subsets. Thus, Mantha does not make obvious claims 4-6. As to claims 5 and 6, Kim discloses puncture table entries (Figure 2) that each contain the same number of bits as other entries.

Claims 7 and 8 recite either "each memory element storing a variable degree" or each memory element storing a variable node location." Applicant's disclosure, on page 9, lines 15-17, recites "In terms of the matrix **H** of Figure 1A, the first puncture sequence may represent either the non-zero element locations (variable node locations) or the number of

non-zero elements (variable degree) of the first column." It does not appear that Mantha discloses or fairly suggests these limitations. Thus, claims 7 and 8 are not made obvious by Mantha.

Also, as to claim 9, Mantha does not appear to disclose or fairly suggest "each memory element storing one of a variable degree, a check degree, a variable node location, or a check node location." Thus, claim 9 is not made obvious by Mantha.

As to claims 22 and 25, Mantha does not disclose "each of S_1, S_2 and S_3 are subsets of S_{max} but not subsets of any of the other of S_1, S_2 and S_3." Thus, claims 22 and 25 are allowable over Mantha for this additional reason.

The Patent Office has not addressed the merits of claims 20-25 in the Office Action mailed August 24, 2005.

The Applicant respectfully requests that the Patent Office review the cited art and rejections in light of the above remarks, and pass each of claims 1-26 to issue. The undersigned representative welcomes the opportunity to resolve any matters that may remain, formal or otherwise, via teleconference at the Patent Office's discretion.

Respectfully submitted:

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